Curriculum Vitae

Robert W. Horst, Ph.D.

Expertise

- Computer design and architecture
- Fault tolerant computing
- CPU, cache and memory design
- I/O and storage subsystems
- High speed networks
- Performance evaluation
- Hardware testing
- Patents and intellectual property

Professional Summary

From: 2001 HT Consulting
To: Present San Jose, CA
Position: Independent consultant

- Work with startups, VC firms, established companies and law firms on architectural definition of new products, design reviews, technical due diligence on potential investments, identification and protection of intellectual property and litigation support.
- Expert witness in patent and technology litigation

From: 2001 Tibion Corporation
To: Present Sunnyvale, CA
Position: Co-Founder and CTO

- Started Tibion to build active orthotic devices for assistance and rehabilitation of those with impaired mobility.
- Initial product conception and early technology investigation
- Development of electronics, software and mechanics for several generations of prototypes
- Design and test of production electronics and control algorithms
- Filed patents and formulated IP strategy

From: 2002 Network Appliance, Inc.
To: 2003 Sunnyvale, CA
Position: Technical Director

- Investigate processor and interconnect options for future generations of network-attached storage subsystems.
- Represent Network Appliance in the PCI Express Advanced Switching working group.

Curriculum Vitae

From: 1999 3ware, Inc.
To: 2001 Mountain View, CA
Position: Vice President, Research & Technology

- Initiate and lead project that resulting in industry's first Ethernet Storage Area Network storage subsystem. Greatly enhance the company's patent position with 10 new patent applications.
- Develop novel disk mirroring architecture and help the company to grow from 15 to over 100 people. Participate in fund raising activities and prototype development.

From: 1980 Tandem Computers / Compaq Computers
To: 1999 Cupertino, CA
Position: Technical Director

- Designer and architect of several generations of fault-tolerant mainframes used in banking, stock exchanges, and commerce.
- Co-founder of Tandem Labs. Initiated internal projects and started several joint research projects with universities,
- Lead architect of the ServerNet System Area Network. Internal and external champion of ServerNet. Wrote technical papers and made numerous presentations to technical audiences and customers
- Principal architect of the NonStop Cyclone superscalar processor. Listed inventor on the industry's first superscalar patents.
- Project leader of NonStop TXP fault-tolerant CPU.

From: 1976 Hewlett-Packard Co.
To: 1980 Cupertino, CA
Position: Development Engineer

- Designed the micro-sequencer and cache of the HP3000 Series 64 processor.
- Designed a test system for the processor cards using pseudo-random scan and signature analysis.

Litigation Support Experience

Served as a testifying expert witness on patent cases related to systems, processors and storage. Served as a consulting expert on class-action and defective product cases. Further details furnished on request.

Patents

#	PAT. NO.	TITLE
73	7,811,189	Deflector Assembly
72	7,648,436	Rotary Actuator
71	7,537,573	Active muscle assistance device and method
69	7,484,038	Method and apparatus to manage storage devices
68	7,468,982	Method and apparatus for cluster interconnection using multi-port nodes and multiple routing fabrics
67	7,365,463	High torque motor
66	7,239,065	Electrostatic actuator with fault tolerant electrode structure
65	6.966,882	Active muscle assistance device and method
64	6.950,428	System and method for configuring adaptive sets of links between routers in a system area network (SAN)
63	6,924,780	Spatial display of disk drive activity data
62	6,775,794	Use of activity bins to increase the performance of disk arrays
61	6,753,878	Parallel pipelined merge engines
60	6,751,757	Disk drive data protection using clusters containing error detection sectors
59	6,650,533	Pluggable drive carrier assembly
58	6,646,984	Network topology with asymmetric fabrics
57	6,631,131	Transpose table biased arbitration scheme
56	6,591,339	Methods and systems for selecting block sizes for use with disk arrays
55	6,591,338	Methods and systems for mirrored disk arrays
54	6,567,892	Use of activity bins to increase the performance of disk arrays
53	6,549,977	Use of deferred write completion interrupts to increase the performance of disk operations
52	6,516,032	First-order difference compression for interleaved image data in a high-speed image compositor
51	6,496,940	Multiple processor system with standby sparing
50	6,487,633	Methods and systems for accessing disks using forward and reverse seeks
49	6,484,235	Methods and systems for dynamically distributing disk array data accesses
48	6,424,655	Transpose table-biased arbitration
47	6,424,523	Pluggable drive carrier assembly
46	6,266,765	Computer architecture capable of execution of general purpose multiple instructions
45	6,233,702	Self-checked, lock step processor pairs
44	6,157,967	Method of data communication flow control in a data processing system using busy/ready commands
43	6,092,177	Computer architecture capable of execution of general purpose multiple instructions

42	6,009,506	Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions
41	5,964,835	Storage access validation to data messages using partial storage address data indexed entries containing permissible address range validation for message source
40	5,930,275	Clock error detection circuit
39	5,918,032	Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions
38	5,914,953	Network message routing using routing table information and supplemental enable information for deadlock prevention
37	5,890,003	Interrupts between asynchronously operating CPUs in fault tolerant computer system
36	5,867,501	Encoding for communicating data and commands
35	5,838,894	Logical, fail-functional, dual central processor units formed from three processor units
34	5,765,007	Microinstruction sequencer having multiple control stores for loading different rank registers in parallel
33	5,758,113	Refresh control for dynamic memory in multiple processor system
32	5,752,064	Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions
31	5,751,932	Fail-fast, fail-functional, fault-tolerant multiprocessor system
30	5,742,135	System for maintaining polarity synchronization during AMI data transfer
29	5,710,549	Routing arbitration for shared resources
28	5,694,121	Latency reduction and routing arbitration for network message routers
27	5,675,579	Method for verifying responses to messages using a barrier message
26	5,628,024	Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions
25	5,574,941	Computer architecture capable of concurrent issuance and execution of general purpose multiple instruction
24	5,574,933	Task flow computer architecture
23	5,404,550	Method and apparatus for executing tasks by following a linked list of memory packets
22	5,390,355	Computer architecture capable of concurrent issuance and execution of general purpose multiple instructions
21	5,384,906	Method and apparatus for synchronizing a plurality of processors
20	5,353,436	Method and apparatus for synchronizing a plurality of processors
19	5,329,629	Apparatus and method for reading, writing, and refreshing memory with direct virtual or physical access
18	5,317,726	Multiple-processor computer system with asynchronous execution of identical code streams
17	5,287,472	Memory system using linear array wafer scale integration architecture
16	5,239,641	Method and apparatus for synchronizing a plurality of processors

15	5,203,005	Cell structure for linear array wafer scale integration architecture with capability to open boundary I/O bus without neighbor acknowledgement
14	5,193,175	Fault-tolerant computer with three independently clocked processors asynchronously executing identical code that are synchronized upon each voted access to two memory modules
13	5,146,589	Refresh control for dynamic memory in multiple processor system
12	5,075,844	Paired instruction processor precise exception handling mechanism
11	5,072,364	Method and apparatus for recovering from an incorrect branch prediction in a processor that executes a family of instructions in parallel
10	5,034,964	N:1 time-voltage matrix encoded I/O transmission system
9	5,016,208	Deferred comparison multiplier checker
8	4,872,109	Enhanced CPU return address stack
7	4,823,252	Overlapped control store
6	4,800,486	Multiple data patch CPU architecture
5	4,754,396	Overlapped control store
4	4,636,943	Enhanced CPU microbranching architecture
3	4,618,956	Method of operating enhanced alu test hardware
2	4,574,344	Entry control store for enhanced CPU pipeline performance
1	4,571,673	Enhanced CPU microbranching architecture

Education

1991	University of Illinois	Ph.D., Computer Science. Design and simulation of a massively parallel, multi-threaded *task flow* computer.
1978	University of Illinois	M.S., Electrical Engineering. Design, construction and debugging of a shared memory parallel microprocessor system.
1975	Bradley University	B.S., Electrical Engineering. Summa Cum Laude.

Publications

Bionics

R. Horst, “A Bio-Robotic Leg Orthosis for Rehabilitation and Mobility Enhancement,” Proc. 31st Annual International Conf. of the IEEE Engineering in Medicine and Biology Society, Sept, 2009.

R. Horst, "FlexCVA: A Continuously Variable Actuator for Active Orthotics," Proc. 28th Annual International Conf. of the IEEE Engineering in Medicine and Biology Society, Aug., 2006.

Fault Tolerance

R. Horst, "Reliable Design of High-speed Cache and Control Store Memories," Proc. 19th Int. Symp. Fault-Tolerant Computing, June 1989.

J. Bartlett, W. Bartlett, R. Carr, D. Garcia, J. Gray, R. Horst, R. Jardine, et al., "Fault Tolerance in Tandem Computer Systems," in Reliable Computer Systems, D. P. Siewiorek and R. S. Swarz, Eds., Bedford, MA: Digital Press, 1992.

R. Horst, D. Jewett, D. Lenoski, "The Risk of Data Corruption in Microprocessor-based Systems," Proc. 23rd International Symposium on Fault-tolerant Computing, June 1993.

R. Horst, "Massively Parallel Systems You Can Trust," COMPCON Digest of Papers, San Francisco, CA, Feb. 28-March 4, 1994.

W. E. Baker, et al., "A Flexible ServerNet-based Fault-Tolerant Architecture," in Proc. 25th Int. Symp. Fault-Tolerant Computing, Pasadena, CA, June 27-30 1995.

CPU Architecture

R. Horst, "A Linear-Array WSI Architecture for Improved Yield and Performance," in Proc. Int. Conf. WSI, San Francisco, CA, pp. 85-91, Jan. 1990.

R. Horst, "Task Flow Computer Architecture," in Proc. Int. Conf. Parallel Processing, Vol. I, pp. 533-540, Aug. 1990.

R. Horst, "Task Flow: A Novel Approach to Fine-grain Wafer-scale Parallel Computing," Coordinated Science Lab. Report CRHC-91-15, University of Illinois, April 1991.

R. Horst, R. Harris, and R. Jardine, "Multiple Instruction Issue in the NonStop Cyclone Processor," in Proc. 17th Int. Symp. Computer Architecture, May 1990.

R. W. Horst, "Task-Flow Architecture for WSI Parallel Processing," Computer, vol. 25, no. 4, pp. 10-18, April 1992.

Storage

J. Gray, B. Horst, and M. Walker, "Parity striping of disk arrays: Low cost reliable storage with acceptable throughput," in Proc. 16th Int. Conf. on Very Large Databases, Brisbane, Australia, pp. 148-161, Aug. 1990.

R. Horst, J. McDonald, B. Alessi, “Beyond RAID: An Architecture for Improving PC Fault Tolerance and Performance, Digest of Fast Abstracts, 29th Int. Symp. Fault-Tolerant Computing, June 1999.

R. Horst, “TwinStor Technology: A Compelling Case for Multiple Drives in PCs, Servers and Workstations,” 3ware Technical Report TR-1999-2, 3ware, Inc., August 1999.

L. Chung, J. Gray, B. Worthington, R. Horst, “Study of Random and Sequential IO on Windows 2000™”, http://research.microsoft.com/BARC/Sequential_IO/.

R. Horst, “Storage Networking: The Killer Application for Gigabit Ethernet,” dmDirect Business Intelligence Newsletter, http://www.dmreview.com. April 20, 2001.

R. Horst, “IP Storage and the CPU Consumption Myth,” proc. IEEE International Symposium on Network Computing and Applications (NCA2001), October 2001.

Networks

R. Horst, "TNet: A Reliable System Area Network," IEEE Micro, vol. 15, no. 1, pp. 37-45, February 1994.

R. Horst, "ServerNet Deadlock Avoidance and Fractahedral Topologies," in Proc. 10th Int'l Parallel Processing Symposium, Honolulu, Hawaii, pp. 274-280, 1995.

R. Horst and D. Garcia, "ServerNet SAN I/O Architecture," Proc. Hot Interconnects V, August 1997.

R. Horst, "A Fault Model for System Area Networks," FTCS-28 Fast Abstract, June 1998.

D.R Avresky, V. Shurbanov, R. Horst, “The effect of router arbitration policy on scalability of ServerNet Topologies,” Microprocessors and Microsystems 21, pp 545-561, 1998.

D.R Avresky, V. Shurbanov, R. Horst, W. Watson, L. Young, D. Jewett. “Performance Modeling of ServerNet SAN Topologies,” Journal of Supercomputing, V. 14, pp. 19-37, 1999.

D.R Avresky, V. Shurbanov, R. Horst, “Optimizing router arbitration in point-to-point networks,” Computer Communications, 22, pp 608-620, 1999.

D.R Avresky, V. Shurbanov, R. Wilkinson, R. Horst, W. Watson, L. Young, “ Maximum delivery time and hot spots in ServerNet topologies, Computer Networks 31, pp. 1891-1910, 1999.

A. Hossain, S. Kang, R. Horst, “ServerNet and ATM Interconnects: Comparison for Compressed Video Transmission,” Journal of Communications and Networks, V. 1 No. 2, June 1999.

Professional Associations and Achievements

IEEE Fellow. Elected "for contributions to the architecture and design of fault tolerant systems and networks," 2001

Compaq Key Patent Award for patent 5,751,932 - Fail-fast, fail-functional, fault-tolerant multiprocessor system, 2002.

Distinguished Alumni Award for "Pioneering Contributions to Fault-tolerant Computer Architecture," University of Illinois department of Electrical and Computer Engineering, 1998.

Daniel A. Slotnick Award for Most Original Paper, ICPP, 1990

Program Committees: Int. Symposium on Fault Tolerant Computing (FTCS) 1991, 1997, 1999. Dependable Systems and Networks (DSN 2002). Int. Symposium on Network Computing and Applications (NCA) 2001, 2003, IEEE Workshop on Fault-Tolerant Parallel, Distributed and Network-Centric Systems 2004, Workshop on System Area Networks 2004.

Tibion Awards:

2005 Grand Prize Winner, Boomer Business Plan Competition.
2008 Silicon Valley Emerging Technology Award (ETA) for Medical Devices
2010 Medical Design Excellence Award (MDEA)